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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,016	01/30/2004	Brady L. Keays	400.228US01	7971

27073 7590 05/01/2007
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	
MAIL DATE	**DELIVERY MODE**
05/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,016	KEAYS, BRADY L.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-102* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-28,36-43,45-62,69-82,84,89-100 and 102* is/are allowed.

6)☒ Claim(s) *1-7,29-33,44,63,64,67,68,83,85-88 and 101* is/are rejected.

7)☒ Claim(s) *34-35 and 65-66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the After-Final Amendment submitted on March 26, 2007 and the IDS submitted on August 16, 2004.

Response to Amendment

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claim 83 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art.

Applicant's admitted prior art discloses reading a physical page row [which includes user sectors and data sectors] from a flash memory; transferring the selected data from the flash memory; masking off a first selected range of data column bit values and writing the selected range of data to a physical row of a target block (section 0043 of the specification).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 29-32, 44, 67, 85-88 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of Applicant's Admitted Prior Art (APA). Regarding claims 1, 29, 44, 69, 85 and 101, Estakhri discloses at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages (sectors) arranged in a plurality of erase blocks, wherein each physical row page containing one or more user data sectors and one or more overhead data areas (Abstract); Estakhri does not disclose a non-split data move control circuit adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy back move operations such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead areas into an internal latch of the at least one non-volatile memory device; transferring the selected data from the selected non-volatile memory device; masking the selected user data sectors and the associated overhead data areas and writing the selected data to a physical page row of a target erase block. However, the APA discloses a non-split data move control circuit (circuitry responsible for performing move operations) adapted to move one or more selected

user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source block to a target block in a modified copy back move operations such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source block are moved to a target physical row page of the target block by reading the selected user data sectors and the associated overhead areas into an internal latch of the at least one non-volatile memory device; transferring the selected data from the selected non-volatile memory device; masking the selected user data sectors and the associated overhead data areas into an internal latch and writing the selected data to a physical page row of a target erase block (section 0043 of the specification). The features disclosed by the APA provides efficiency by allowing the system to specifically extract and move the data needed or desired from the remaining data. One of ordinary skill in the art would have been motivated to allow the system to copy/move portions of data and would have been motivated to use the teachings of the admitted prior art with the system taught by Estakhri for the desirable purpose of flexibility and efficiency.

Regarding claims 2, 31, 86, 88 Estakhri discloses a mass storage device compatible interface to the non-volatile memory system (Estakhri, C 1, L 19-40).

Regarding claim 3, Estakhri disclose the non-volatile memory system having a PCMCIA-ATA compatible interface (Estakhri, C 4, L 41-43).

Regarding claims 4 and 30, the system derived from Estakhri and the APA discloses a NAND architecture Flash memory device (APA, section 0043).

Regarding claim 5, Estakhri discloses the user data sector containing 512 bytes (Estakhri, C 2, L 61-64).

Regarding claims 6 and 32, Estakhri discloses each overhead data area containing an error correction code (ECC)(Estakhri, C 2, L 40-42).

Regarding claims 67 and 98, Estakhri and the APA do not disclose masking out a selected range of data by inserting logical l's. However, it is well known in the art to perform masking by inserting logical 1's and such functionality is a simple mechanism for masking out data. Thus it would have been obvious to one of ordinary skill in the art to mask out the selected bits in the system taught by Estakhri and the APA by inserting logical 1's for the desirable purpose of simplicity.

Regarding claim 87, Estakhri disclose the host comprising a processor and external memory controller (Estakhri, C 4, L 14-15).

7. Claims 7 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of the APA as applied to claim 1 above and further in view of Danilak (USPN: 7,117,421).

Estakhri and the APA disclose ECC codes but they do not explicitly disclose evaluating the ECC codes as data is moved. Danilak discloses evaluating ECC codes as data is being moved (C 7, L 47-50; C 8, L 20-22, 28-32). This feature taught by Danilak provides reliability by ensuring that the data moved is accurate. Hence, it would have been obvious to one of ordinary skill in the art to evaluate the ECC codes as the data is moved in the system taught by Estakhri and the APA for the desirable purpose of reliability.

8. Claims 63-64 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art.

Regarding claims 63-64, Applicant's admitted prior art discloses reading a physical page row of a source block from a flash memory; transferring the selected data from the flash memory; masking off a first selected range of data column bit values and writing the selected range of data to a physical row of a target block (section 0043 of Applicant's specification). The admitted prior discloses a source block and a target block, however, the blocks are not a source erase block and a target erase block. The admitted prior art executes the above features when performing a data move operation wherein a subset of data read from a source block is written/moved to a target block, which provides efficiency since only the desired data is moved instead of the entire block. However, erase blocks are well known in the art in flash memory devices. Hence, it would have been obvious to one of ordinary skill in the art to perform the above features for erase blocks wherein only the desired data is erased instead of the entire source erase block, since only the selected masked data/overhead is moved to a target block, for the desirable purpose of efficiency.

9. Claims 63-64, 68 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al (PGPUB: US 2004/0193774) in view of Applicant's Admitted Prior Art.

Regarding claims 63 and 83, Iwata discloses reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices (section 0028, lines 2-4; section 0153); transferring the selected data from the selected non-volatile memory device and writing the selected data to a physical page row of a target erase block (section 0028, lines 4-10). Iwata does not disclose masking off a first selected range of column bit values. However, Applicant's admitted prior art teaches the concept of selecting a portion of data by masking the data (section 0043 of Applicant's specification). This feature taught by the admitted prior art provides efficiency by allowing the system to specifically extract the data needed or desired from the remaining data. In Iwata's system the entire read data is transferred and written into a target block. However, in other situations it may be desirable to write portions of the read data and not the entire amount of data read. One of ordinary skill in the art would have been motivated to allow the system to write portions of data and would have been motivated to use the teachings of the admitted prior art with the system taught by Iwata for the desirable purpose of flexibility and efficiency.

Regarding claims 64, Iwata disclose a NAND architecture Flash memory device (Iwata, section 0095).

Regarding claim 68, Iwata disclose a mass storage device compatible interface to the non-volatile memory system (Iwata, sections 0002 and 0003).

Allowable Subject Matter

10. Claims 8-28, 36-43, 45-62, 69-82, 84, 89-100 and 102 are allowed.

11. Claims 34-35 and 65-67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

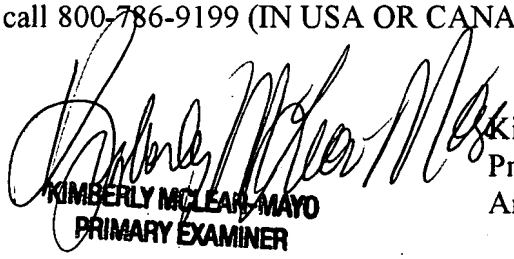
13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Estakhri – USPN: 7, 155, 559 – segregating data and overhead in flash memory.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Monday-Friday (10-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

April 17, 2007